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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
09/909,013	07/19/2001	Makoto Yoshino	TIJ-29448	8724

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
GEYER, SCOTT B

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,013	YOSHINO ET AL.	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10,12,14,15 and 17-19* is/are rejected.

7)☒ Claim(s) *11,13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art.

3. As to ***claim 5***, applicant's prior art figure 10 discloses a thermoplastic film (110) used as a substrate for carrying semiconductor chips. The film has two rows of sprocket holes (112), each row disposed along an edge of the film. The film also has a plurality of through holes (as stated in specification page 1, line 30, but not depicted in figure 10) which are situated under circuit patterns (114). The circuit patterns (114), and thus the through holes, are situated between the two rows of sprocket holes (112).

4. As to ***claim 6***, applicant's figure 10 discloses multiple sprocket holes (112) which thus must have a certain pitch **L**, and a plurality of through holes (not pictured) which thus must have a pitch **p**. Further, as neither **n**, **m**, **L** or **p** are defined by the specification, drawings or claims, any two integers n and **m**, where **n<m**, could satisfy the equation (**m*p**)=(**n*L**).

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Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 7, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Cho (6,235,555).

7. As to ***claim 7***, Applicant's admitted prior art teach an insulation film used as a substrate for semiconductor devices as shown above in paragraph 12. Applicant's disclosed prior art further teach sprocket and through holes. Applicant's admitted prior art does not specifically teach forming through holes along a transverse direction in a region between sprocket holes, and moving the insulation film in a length-wise direction. However, Cho teach sprocket holes used to (figure 9, numeral 71) formed along both sides of the insulation film, i.e. reel-deployed printed circuit board (70). The sprocket holes are sued to advance the film along, in combination with toothed sprocket mechanism. As the film is advanced, through holes are formed in the film (column 4, line 22 et seq.). Also, since neither **n** nor **L** are defined by applicant's specification, drawings or claims, the sprockets as disclosed by Cho also have a pitch **L**, and they are moved a length **n*L** by the sprocket tooth mechanism. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by applicant's admitted prior art with a mechanism to move the film and form through holes as taught by Cho. The sprocket holes are used to assist in consistent advancing of the film through manufacturing steps, so that all other through holes necessary for manufacturing may also be made consistently.

8. As to ***claim 8***, applicant's admitted prior art teach forming circuit patterns (figure 10, numeral 114) and conductor patterns (116) on the film, which are connected (specification page 2, lines 1-4).

9. As to ***claim 12***, applicant's admitted prior art teach forming circuit patterns (figure 10, numeral 114) on the film and bonding a semiconductor chip to the circuit pattern formed (specification page 2, lines 14 et seq.). Applicant's admitted prior art also teach forming conductor patterns (116) on the film and electrically connecting the circuit patterns and the conductor patterns (specification page 2, lines 1-4).

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10. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art.

11. As to ***claim 9***, applicant's prior art figure 10 discloses a thermoplastic film (110) used as a substrate for carrying semiconductor chips. The film has two rows of sprocket holes (112), each row disposed along an edge of the film. The film also has a plurality of through holes (as stated in specification page 1, line 30, but not depicted in figure 10) which are situated under circuit patterns (114). The circuit patterns (114), and thus the through holes, are situated between the two rows of sprocket holes (112). Applicant's figure 10 discloses multiple sprocket holes (112) which thus must have a certain pitch **L**, and a plurality of through holes (not pictured) which thus must have a pitch **p**. Also, applicant's admitted prior art teach forming circuit patterns (figure 10, numeral 114) and conductor patterns (116) on the film, which are connected (specification page 2, lines 1-4). The circuit patterns have main lines which cross over the entire section of film depicted by figure 10. Applicant's admitted prior art also teach mounting a chip onto the film, sealing with a molding compound and punching out individual packages (specification page 2, line 14 et seq.). Applicant's admitted prior art

does not disclose a 'sub-line' electrically connecting the circuit patterns to the conductor patterns. However, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method as disclosed by applicant's admitted prior art with a 'sub-line' to provide electrical connection between the conductor pattern and the circuit pattern, as applicant's admitted prior art does disclose that such a connection between the two does exist.

12. As to ***claim 10***, applicant's admitted prior art teach a plating step using conductor patterns (116) and bridge (118) (see specification page 2, line 3 et seq.).

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13. Claims 14, 15, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Cho (6,235,555).

14. As to ***claim 14***, applicant's prior art figure 10 discloses a thermoplastic film (110) used as a substrate for carrying semiconductor chips. The film has two rows of sprocket holes (112), each row disposed along an edge of the film. The film also has a plurality of through holes (not depicted, as stated in specification page 1, line 30) which are situated under circuit patterns (114). The circuit patterns (114), and thus the through holes, are situated between the two rows of sprocket holes (112). Applicant's admitted prior art also recites mounting a semiconductor chips over through holes, sealing the chip in resin and using a punch-out jig to removing the package from the insulation film to provide a complete packaged chip. Applicant does not specifically teach cutting the insulating film to However, Cho teaches a reel printed flexible circuit board 68 in figure 9 wherein semiconductor chips 21 are attached to the flexible base

and are covered in encapsulant 24. These process steps are also taught in figure 13 which further teaches separating the individual packages form the reel printed circuit board (step 95) by cutting (see also column 6, lines 45 et seq.). At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method as taught by the applicant's admitted prior art with chip attachment, encapsulation and separation as taught by Cho so as to provide a complete process for providing completed individual semiconductor chips protected by encapsulant.

15. As to ***claim 15***, applicant's prior art figure 10 discloses a thermoplastic (insulation) film (110) used as a substrate for carrying semiconductor chips. The film has two rows of sprocket holes (112), each row disposed along an edge of the film. The film also has a plurality of through holes (not depicted, as stated in specification page 1, line 30) which are situated under circuit patterns (114). Applicant's figure 10 discloses multiple sprocket holes (112) which thus must have a certain pitch **L**, and a plurality of through holes (not pictured) which thus must have a pitch **p**. The circuit patterns (114), and thus the through holes, are situated between the two rows of sprocket holes (112).

16. As to ***claim 17***, applicant's prior art figure 10 discloses a thermoplastic (insulation) film (110) used as a substrate for carrying semiconductor chips. The film has two rows of sprocket holes (112), each row disposed along an edge of the film. The film also has a plurality of through holes (not depicted, as stated in specification page 1, line 30) which are situated under circuit patterns (114). Applicant's figure 10 discloses multiple sprocket holes (112) which thus must have a certain pitch **L**, and a plurality of

through holes (not pictured) which thus must have a pitch **p**. The circuit patterns (114), and thus the through holes, are situated between the two rows of sprocket holes (112).

17. As to ***claim 19***, applicant's admitted prior art teach plating the entire surface of the insulating film with metal after the through holes have been formed (see specification page 1, line 24 through page 2, line 13).

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18. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art and Cho (6,235,555) as applied to claim 14 above, and further in view of Hashimoto (6,200,824 B1).

19. As to ***claim 18***, applicant's admitted prior art teach plating the entire surface of the insulating film with metal after the through holes have been formed (see specification page 1, line 24 through page 2, line 13). Neither applicant's admitted prior art nor Cho specifically teach solder being plated in through holes. However, Hashimoto teaches through holes in a tape carrier 10 and through holes 18 are formed in the tape carrier (figure 2A). The through holes allow solder balls to be positioned on one side of the tape carrier and extend through to complete an electrical connection to the other side of the tape carrier (column5, lines 25-67). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the method of Applicant's admitted prior art and Cho with solder balls as taught by Hashimoto as solder balls are notoriously well known in the art for completing electrical connections in semiconductor devices.

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Allowable Subject Matter

20. Claims 11, 13 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11, 13 and 16, which depend on independent claim 9 and 10 respectively, teach a dicing step wherein the dicing blade has a blade trim width which is wider than the wiring width of the 'sub-line' of the conductor pattern and the 'sub-line' is not left behind on the insulation film after the dicing step has been performed. The cited prior art does not teach dicing using a dicing blade having a blade width wider than the wiring width of the 'sub-line'.

Response to Arguments

21. Applicant's arguments filed 2-5-03 have been fully considered but they are not persuasive. Applicant has argued that that the admitted prior art does not imply a two-dimensional plurality of through holes at a pitch **p**. However, applicant's prior does explicitly recite "beneath the region of this circuit pattern **114**, multiple through holes are formed prior to formation of this circuit (see page 1, lines 29 and 30). Therefore, by the admission of having "*multiple through holes*" this does imply at least two holes in the film, and therefore, two holes in a film are spaced two-dimensionally from one another and therefore define an array. Further, since at least two holes exist, they do have a pitch **p** from one another by applicant's use of the word "pitch". Furthermore, since the claims are silent as to any exact value for **p**, and only submit a pitch **p** as a random variable, it is thus inherent from applicant's disclosure that the "*multiple through holes*"

also have a pitch **p**. In summary, the lack of any value or definition for **m**, **n**, **p**, **L**, and '*array*' in the claims necessitates the rejection of these claims over the cited prior art, since the claimed subject matter is too broad to patentably distinguish over the prior art.

Conclusion

22. This is a continuation of applicant's earlier Application No. 09/909,013. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SCOTT GEYER
PATENT EXAMINER

S.B.G.
April 1, 2003